## CS 33

## Exploiting Caches

## E-way Set-Associative Cache (Here: E = 2)

E = 2: two lines per set
Assume: cache block size 8 bytes
Address of short int:


## E-way Set-Associative Cache (Here: E = 2)

E = 2: two lines per set
Assume: cache block size 8 bytes
Address of short int:


## No match:

- One line in set is selected for eviction and replacement
- Replacement policies: random, least recently used (LRU), ...


## Quiz 1

| 100 | 01 | 100 |
| :---: | :---: | :---: |

0 | $v$ |  |  |  |  |  |  |  |  |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- |
| $\mathrm{tag}=0$ |  |  |  |  |  |  |  |  |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |

| $v$ |  |  |  |  |  |  |  |  |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- |
|  | tag=2 |  |  |  |  |  |  |  |
| 2 | 2 | 2 | 2 | 2 | 3 | 3 | 3 | 3 |



| $v \quad$ tag=4 |  |  |  |  |  |  |  |  |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- |
| 6 | 6 | 6 | 6 | 6 | 7 | 7 | 7 | 7 |



| v tag=3 |  |  |  |  |  |  |  |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- |
| $a$ | $a$ | $a$ | $a$ | $b$ | $b$ | $b$ | $b$ |


| v tag=a$e$ $e$ $e$$e^{\prime}$ | $f$ | $f$ | $f$ | $f$ |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- |

Given the address above and the cache contents as shown, what is the value of the int at the given address?
a) 1111
b) 3333
c) 4444
d) 7777

## 2-Way Set-Associative Cache Simulation

| $t=2$ | $s=1$ | $b=1$ |
| :---: | :---: | :---: |
| $x x$ | $x$ | $x$ |

$\mathrm{M}=16$ byte addresses, $\mathrm{B}=2$ bytes/block, S=2 sets, E=2 blocks/set

Address trace (reads, one byte per read):

| 0 | $\left[\mathrm{OOOO}_{2}\right]$, | miss |
| :--- | :--- | :---: |
| 1 | $\left[00 \mathrm{O} 1_{2}\right]$, | hit |
| 7 | $\left[011_{2}\right]$, | miss |
| 8 | $\left[\mathrm{HOO}_{2}\right]$, | miss |
| 0 | $\left[00 \mathrm{OO}_{2}\right]$ | hit |


|  | v | Tag | Block |
| :---: | :--- | :--- | :--- |
| Set 0 | 1 | 00 | $M[0-1]$ |
|  | 1 | 10 | $M[8-9]$ |
|  |  |  |  |

Set 1 |  | 1 | 01 |
| :--- | :--- | :--- |
|  |  | $M[6-7]$ |
|  |  |  |

## A Higher-Level Example

}

```
```

```
int sum_array_rows(double a[16][16])
```

```
int sum_array_rows(double a[16][16])
{
{
    int i, j;
    int i, j;
    double sum = 0;
    double sum = 0;
    for (i = 0; i < 16; i++)
    for (i = 0; i < 16; i++)
        for (j = 0; j < 16; j++)
        for (j = 0; j < 16; j++)
        sum += a[i][j];
        sum += a[i][j];
    return sum;
```

    return sum;
    ```
```

int sum_array_rows(double a[16][16])
{
int i, j;
double sum = 0;
for (j = 0; j < 16; i++)
for (i = 0; i < 16; j++)
sum += a[i][j];
return sum;
}

```
assume: cold (empty) cache, a[0][0] goes here


\section*{A Higher-Level Example}
```

int sum_array_rows(double a[16][16])
{
int i, j;
double sum = 0;
for (i = 0; i < 16; i++)
for (j = 0; j < 16; j++)
sum += a[i][j];
return sum;
}

```

\begin{tabular}{|l|l|l|l|l|l|l|l|}
\hline\(a_{0,0}\) & \(a_{0,1}\) & \(a_{0,2}\) & \(a_{0,3}\) & \(a_{1,0}\) & \(a_{1,1}\) & \(a_{1,2}\) & \(a_{1,3}\) \\
\hline \hline\(a_{0,4}\) & \(a_{0,5}\) & \(a_{0,6}\) & \(a_{0,7}\) & \(a_{1,4}\) & \(a_{1,5}\) & \(a_{1,6}\) & \(a_{1,7}\) \\
\hline \hline\(a_{0,8}\) & \(a_{0,9}\) & \(a_{0,10}\) & \(a_{0,11}\) & \(a_{1,8}\) & \(a_{1,9}\) & \(a_{1,10}\) & \(a_{1,11}\) \\
\hline \begin{tabular}{lllllll}
\(a_{0,12}\) & \(a_{0,13}\) & \(a_{0,14}\) & \(a_{0,15}\) & \(a_{1,12}\) & \(a_{1,13}\) & \(a_{1,14}\) \\
\hline
\end{tabular} & \(a_{1,15}\) \\
\hline
\end{tabular}

return sum;

\section*{A Higher-Level Example}
int sum_array_cols(double a[16][16])
int sum_array_cols(double a[16][16])
{
{
    int i, j;
    int i, j;
    double sum = 0;
    double sum = 0;
    for (j=0; i < 16; i++)
    for (j=0; i < 16; i++)
        sum += a[i][j];
        sum += a[i][j];
    return sum;
    return sum;
}
}


\section*{Conflict Misses}
```

double dotprod(double x[8], double y[8]) {
double sum = 0.0;
int i;
for (i=0; i<8; i++)
sum += x[i] * y[i];
return sum;
}

```

\section*{Intel Core i5 and i7 Cache Hierarchy}

\section*{Processor package}


\section*{What About Writes?}
- Multiple copies of data exist:
- L1, L2, main memory, disk
- What to do on a write-hit?
- write-through (write immediately to memory)
- write-back (defer write to memory until replacement of line)
" need a dirty bit (line different from memory or not)
- What to do on a write-miss?
- write-allocate (load into cache, update line in cache)
» good if more writes to the location follow
- no-write-allocate (writes immediately to memory)
- Typical
- write-through + no-write-allocate
- write-back + write-allocate

\section*{Accessing Memory}
- Program references memory (load)
- if not in cache (cache miss), data is requested from RAM
» fetched in units of 64 bytes
- aligned to 64-byte boundaries (low-order 6 bits of address are zeroes)
» if memory accessed sequentially, data is pre-fetched
» data stored in cache (in 64-byte cache lines)
- stays there until space must be re-used (least recently used is kicked out first)
- if in cache (cache hit) no access to RAM needed
- Program modifies memory (store)
- data modified in cache
- eventually written to RAM in 64-byte units

\section*{Cache Performance Metrics}
- Miss rate
- fraction of memory references not found in cache (misses / accesses) = 1 - hit rate
- typical numbers (in percentages):
» 3-10\% for L1
» can be quite small (e.g., < 1\%) for L2, depending on size, etc.
- Hit time
- time to deliver a line in the cache to the processor
» includes time to determine whether the line is in the cache
- typical numbers:
» 1-2 clock cycles for L1
» 5-20 clock cycles for L2
- Miss penalty
- additional time required because of a miss
» typically 50-200 cycles for main memory (trend: increasing!)

\section*{Hits vs. Misses}
- Huge difference between hit and miss times
- could be 100x, if just L1 and main memory
- \(99 \%\) hit rate is twice as good as \(97 \%\) !
- consider:
cache hit time of 1 cycle
miss penalty of 100 cycles
- average access time: 97\% hits: .97 * 1 cycle +0.03 * 100 cycles \(\approx 4\) cycles
\(99 \%\) hits: .99 * 1 cycle +0.01 * 100 cycles \(\approx 2\) cycles
- This is why "miss rate" is used instead of "hit rate"

\section*{Locality}
- Principle of Locality: programs tend to use data and instructions with addresses near or equal to those they have used recently
- Temporal locality:

- recently referenced items are likely to be referenced again in the near future
- Spatial locality:

- items with nearby addresses tend to be referenced close together in time

\section*{Locality Example}
```

sum = 0;
for (i = 0; i < n; i++)
sum += a[i];
return sum;

```
- Data references
- reference array elements in succession (stride-1 reference

Spatial locality pattern)
- reference variable sum each iteration Temporal locality
- Instruction references
- reference instructions in sequence.

Spatial locality
- cycle through loop repeatedly

Temporal locality

\section*{Quiz 2}

Does this function have good locality with respect to array \(a\) ? The array \(a\) is \(\mathbf{M x N}\).
a) yes
b) no
```

int sum_array_cols(int N, int a[][N]) {
int i, j, sum = 0;
for (j = 0; j < N; j++)
for (i = 0; i < M; i++)
sum += a[i][j];
return sum;

```

\section*{Writing Cache-Friendly Code}
- Make the common case fast
- focus on the inner loops of the core functions
- Minimize the misses in the inner loops
- repeated references to variables are good (temporal locality)
- stride-1 reference patterns are good (spatial locality)

\section*{Matrix Multiplication Example}
- Description:
- multiply \(\mathbf{N} \times \mathbf{N}\) matrices
» each element is a double
\(-\mathbf{O}\left(\mathbf{N}^{3}\right)\) total operations
- \(\mathbf{N}\) reads per source element
- \(\mathbf{N}\) values summed per destination
» but may be able to hold in register
```

f* ijk */ 隹 (i=0; i<n; i++) i ild in register
for (j=0; j<n; j++) {
sum = 0.0;
for (k=0; k<n; k++)
sum += a[i][k] * b[k][j];
c[i][j] = sum;
}
}

```
/* ikj */
for (i=0; \(i<n ; i++)\{\)
    for ( \(k=0\); \(k<n\); \(k++\) ) \{
        r = a[i][k];
        for ( \(j=0 ; j<n ; j++\) )
        c[i][j] += r * b[k][j];
    \}
\}

\section*{Miss-Rate Analysis for Matrix Multiply}
- Assume:
- Block size = 64B (big enough for eight doubles)
- matrix dimension ( \(N\) ) is very large
- cache is not big enough to hold multiple rows
- Analysis method:
- look at access pattern of inner loop


\section*{Layout of C Arrays in Memory (review)}
- C arrays allocated in row-major order
- each row in contiguous memory locations
- Stepping through columns in one row:
- for (i \(=0 ; i<N\); \(i++\) )
sum \(+=a[0][i] ;\)
- accesses successive elements
- if block size \((B)>8\) bytes, exploit spatial locality
» compulsory miss rate \(=8\) bytes \(/\) Block
- Stepping through rows in one column:
- for (i \(=0 ; i<n ; i++\) )
sum \(+=\) a[i][0];
- accesses widely separated elements
- no spatial locality!
» compulsory miss rate \(=1\) (i.e. \(100 \%\) )

\section*{Matrix Multiplication (ijk)}
```

/* ijk */
for (i=0; i<n; i++) {
for (j=0; j<n; j++) {
sum = 0.0;
for (k=0; k<n; k++)
sum += a[i][k] * b[k][j];
c[i][j] = sum;
}
}

```

Row-wise
Column-


C


Fixed wise

Misses per inner loop iteration:
\[
\begin{array}{ccc}
\underline{\mathrm{A}} & \underline{\mathrm{~B}} & \underline{\mathrm{C}} \\
0.125 & 1.0 & 0.0
\end{array}
\]

\section*{Matrix Multiplication (jik)}


Misses per inner loop iteration:


\section*{Matrix Multiplication (kij)}
```

/* kij */
for (k=0; k<n; k++) {
for (i=0; i<n; i++) {
r = a[i][k];
for (j=0; j<n; j++)
c[i][j] += r * b[k][j];
}
}

```

Inner loop:


Misses per inner loop iteration:
A
0.0
0.125
C
0.125

\section*{Matrix Multiplication (ikj)}
```

/* ikj */
for (i=0; i<n; i++) {
for (k=0; k<n; k++) {
r = a[i][k];
for (j=0; j<n; j++)
c[i][j] += r * b[k][j];
}
}

```

Inner loop:

Fixed



Row-wise Row-wise

Misses per inner loop iteration:
\begin{tabular}{ccc}
\(\underline{\mathrm{A}}\) & \(\underline{\mathrm{B}}\) & \(\underline{\mathrm{C}}\) \\
0.0 & 0.125 & 0.125
\end{tabular}

\section*{Matrix Multiplication (jki)}


Inner loop:


Misses per inner loop iteration:


\section*{Matrix Multiplication (kji)}
```

/* kji */
for (k=0; k<n; k++) {
for (j=0; j<n; j++) {
r = b[k][j];
for (i=0; i<n; i++)
c[i][j] += a[i][k] * r;
}
}

```

Misses per inner loop iteration:
\begin{tabular}{ccc}
\(\underline{\mathrm{A}}\) & \(\underline{\mathrm{B}}\) & \(\underline{\mathrm{C}}\) \\
1.0 & 0.0 & 1.0
\end{tabular}

\section*{Summary of Matrix Multiplication}
```

for (i=0; i<n; i++)
for (j=0; j<n; j++) {
sum = 0.0;
for (k=0; k<n; k++)
sum += a[i][k] * b[k][j];
c[i][j] = sum;
}

```
```

```
for (k=0; k<n; k++)
```

```
for (k=0; k<n; k++)
    for (i=0; i<n; i++) {
    for (i=0; i<n; i++) {
    r = a[i][k];
    r = a[i][k];
    for (j=0; j<n; j++)
    for (j=0; j<n; j++)
        c[i][j] += r * b[k][j];
        c[i][j] += r * b[k][j];
    }
```

```
    }
```

```
ijk (\& jik):
- 2 loads, 0 stores
- misses/iter = \(\mathbf{1 . 1 2 5}\)
kij (\& ikj):
- 2 loads, 1 store
- misses/iter = 0.25
```

for (j=0; j<n; j++)
for (k=0; k<n; k++) {
r = b[k][j];
for (i=0; i<n; i++)
c[i][j] += a[i][k] * r;
}

```
jki (\& kji):
- 2 loads, 1 store
- \(\mathrm{misses} /\) iter \(=2.0\)

\section*{Core i7 Matrix Multiply Performance}


\section*{In Real Life}
- Multiply two \(1024 \times 1024\) matrices of doubles on sunlab machines
-ijk
» 4.185 seconds
\(-\mathbf{k i j}\)
» 0.798 seconds
-jki
» 11.488 seconds

\section*{Concluding Observations}
- Programmer can optimize for cache performance
- organize data structures appropriately
- All systems favor "cache-friendly code"
- getting absolute optimum performance is very platform specific
» cache sizes, line sizes, associativities, etc.
- can get most of the advantage with generic code
» keep working set reasonably small (temporal locality)
» use small strides (spatial locality)

\section*{CS 33}

\section*{Architecture and the OS}

\section*{The Operating System}


\section*{Processes}
- Containers for programs
- virtual memory
» address space
- scheduling
» one or more threads of control
- file references
» open files
- and lots more!

\section*{Idiot Proof ...}


\section*{Fair Share}


\section*{Architectural Support for the OS}
- Not all instructions are created equal ...
- non-privileged instructions
» can affect only current program
- privileged instructions
» may affect entire system
- Processor mode
- user mode
» can execute only non-privileged instructions
- privileged mode
» can execute all instructions

\section*{Which Instructions Should Be Privileged?}
- I/O instructions
- Those that affect how memory is mapped
- Halt instruction
- Some others ...

\section*{Who Is Privileged?}
- No one
- user code always runs in user mode
- The operating-system kernel runs in privileged mode
- nothing else does
- not even super user on Unix or administrator on Windows

\section*{Entering Privileged Mode}
- How is OS invoked?
- very carefully ...
- strictly in response to interrupts and exceptions
- (booting is a special case)

\section*{Interrupts and Exceptions}
- Things don't always go smoothly ...
- I/O devices demand attention
- timers expire
- programs demand OS services
- programs demand storage be made accessible
- programs have problems
- Interrupts
- demand for attention from external sources
- Exceptions
- executing program requires attention

\section*{Exceptions}
- Traps
- "intentional" exceptions
" execution of special instruction to invoke OS
- after servicing, execution resumes with next instruction
- Faults
- a problem condition that is normally corrected
- after servicing, instruction is re-tried
- Aborts
- something went dreadfully wrong ...
- not possible to re-try instruction, nor to go on to next instruction

\section*{Actions for Interrupts and Exceptions}
- When interrupt or exception occurs
- processor saves state of current thread/process on stack
- processor switches to privileged mode (if not already there)
- invokes handler for interrupt/exception
- if thread/process is to be resumed (typical action after interrupt)
» thread/process state is restored from stack
- if thread/process is to re-execute current instruction
» thread/process state is restored, after backing up instruction pointer
- if thread/process is to terminate
» it's terminated

\section*{Interrupt and Exception Handlers}
- Interrupt or exception invokes handler (in OS)
- via interrupt and exception vector
» one entry for each possible interrupt/exception
- contains
- address of handler
- code executed in privileged mode
» but code is part of the OS
\begin{tabular}{|c|c|}
\hline intrpt/excp & \\
\hline \multirow[t]{7}{*}{} & handler 0 addr \\
\hline & handler 1 addr \\
\hline & handler 2 addr \\
\hline & ... \\
\hline & handler i addr \\
\hline & ... \\
\hline & handler \(\mathrm{n}-1\) addr \\
\hline
\end{tabular}

\section*{handler i}

\section*{Entering and Exiting}
- Entering/exiting interrupt/exception handler more involved than entering/exiting a function
- must deal with processor mode
» switch to privileged mode on entry
» switch back to previous mode on exit
- interrupted process/thread's state is saved on separate kernel stack
- stack in kernel must be different from stack in user program
» why?

\section*{One Stack Per Mode}
\begin{tabular}{|c|c|}
\hline Frame 1 \\
\hline Frame 2 \\
\hline Frame 3 & \\
\hline & \begin{tabular}{c} 
Intrp/Excp \\
Frame
\end{tabular} \\
\hline & Frame 4 \\
\hline & \\
\hline & \\
Frame 5 \\
& \\
\hline
\end{tabular}

\section*{Quiz 3}

If an interrupt occurs, which general-purpose registers must be pushed onto the kernel stack?
a) all
b) none
c) callee-save registers
d) caller-save registers```

